REMARKS

Summary of the Office Action

Claims 5, 18, 20, 22, 27 and 32 are rejected.

The Office Actions rejects claim 32 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, and rejects claims 5, 18, 20, 22, 27 and 32 under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) and Tsutsui (US 7,196,701).

Summary of the Response to the Office Action

Applicant has amended claims 5, 18, 22, 27 and 32 to further define the invention. No new matter has been added. Reexamination and reconsideration of the pending claims are respectfully requested.

Rejection Under 35 U.S.C 102(e)

Claim 5 is allowable over the cited references in that claim 5 recites a combination of elements including, for example, "taking a power source voltage having a constant level of less than 2.9V from a power source of a system".

Claim 18 is allowable over the cited references in that claim 18 recites a combination of elements including, for example, "a power source of a system for generating a power source voltage having a constant level under 2.9V".

Claim 22 is allowable over the cited references in that claim 22 recites a combination of elements including, for example, "generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit ;

supplying the second power source voltage less than 2.9V to the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit for

processing digital signal of the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit".

Claim 27 is allowable over the cited references in that claim 27 recites a combination of elements including, for example, "providing a power source voltage from a power source of a system wherein the power source voltage has a constant level of less than 2.9V".

Claim 32 is allowable over the cited references in that claim 32 recites a combination of elements including, for example, "supplying the first power source voltage of 3.3V to the data driving circuit and the gate driving circuit for processing digital signal of the data driving circuit and the gate driving circuit; generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit; supplying the second power source voltage less than 2.9V to the interface circuit and the timing controller for processing digital signal of the interface circuit and the timing controller".

Regarding claims 5, 18, 22, 27 and 32, the Office Action states notes that Tsutsui uses 3V as the poser saving example.

According to Tsutsui, VDD2 is changed according to a normal operation mode and a power saving mode. In the normal operation mode, VDD2 is changed from 3V to 5V. In the power saving mode, VDD2 is changed from 5V to 3V. In other words, VDD2 does not have a constant level.

On the contrary, power source voltage CVCC of the invention has a constant level of less than 2.9V input from a power source of a system. In addition, the power source voltage CVCC

regarding claim 22, the Office Action states that AAPA discloses supplying the first power voltage less than 3.0V to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit.

According to AAPA, VCC of 3.3V clearly is supplied to elements 11-14.

In the meantime, the Office Action states that claim 33 contains subject matter which was not described in the specification.

The paragraph [0042] of the specification states the following.

[0042] A voltage reducing circuit 7 reduces the VCC voltage of 3.3V supplied from the power source of the system 10 to provide a reduced voltage to the digital circuit devices, such as the interface circuit 1, the timing controller 2, the data driving circuit 3 and the gate driving circuit 4, which recognize a logic high value and a logic low value of the digital signal supplied thereto. The voltage reducing circuit 7, which is comprised of a pulse width modulator, a pulse frequency modulator, a regulator, a low drop out controller, a resistance, a capacitor, etc., reduces the VCC voltage. The voltage reducing circuit 7 may reduce the power source voltage necessary to only a part of digital circuit devices. For example, the voltage reducing circuit 7 may supply the reduced CVCC voltage to the interface circuit 111 and the timing controller 112 while directly supplying the VCC voltage to the data driving circuit 113 and the gate driving circuit 114 without reducing the VCC voltage.

Thus, there is support in the specification where the no reduced voltage is supplied to the drivers and a reduced voltage is supplied to the inferface and timing circuits.

None of the cited reference, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that

claims 5, 18, 22, 27 and 32 and claim 20, which depend therefrom, are allowable over the cited references.

Conclusion

In view of the foregoing, Applicant respectfully requests reconsideration and the timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of the Amendment, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

EXCEPT for issue fees payable under 37 C.F.R. 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due 37 C.F.R. 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No 50-0310. This paragraph is intended to be **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. 1.136(a)(3).

Respectfully submitted,

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